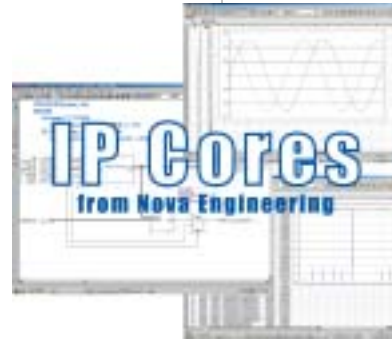


IP Cores

IP Cores are cost-efficient and powerful solutions to common communication development needs. Nova Engineering utilizes its unparalleled expertise in VHDL-based communication system development to provide robust, proven solutions that dramatically save development time and money.

Save development time with proven VHDL solutions

- ▼ High-speed signal processing and communications functions
- ▼ Proven performance with no-risk evaluation
- ▼ Cost-efficient and customizable
- ▼ Low-risk ASIC migration path
- ▼ VHDL source code available



Nova Engineering's IP Cores are modular DSP algorithms and functional blocks for use in custom PLD or ASIC designs. The extensive IP Cores library includes essential components for digital communication and signal processing products, such as digital filters, modulators, complex multipliers, digital synthesizers, correlators, and synchronizers. Written in the industry-standard language of VHDL, IP Cores offer standardized documentation and design portability.

As communication system building blocks, IP Cores can either be linked together or used separately, depending on the application and the amount of complexity required. IP Cores such as the Digital IF Receiver and the Digital Modulator are nearly complete solutions, while the Numerically Controlled Oscillator (NCO) and Complex Multiplier/Mixer cores are less complex, yet extremely versatile. IP Cores are designed with flexibility in mind, allowing designers to upgrade PLDs without the need to completely turn entire new boards.

Nova Engineering participates in Altera's OpenCore Evaluation Program, which allows customers pre-purchase verification of the entire IP Cores line. Nova Engineering is also a Premier Member of Altera's Megafunction Partners Program (AMPP).

Applications

- ▼ Wireless Data Transceivers
- ▼ WLL Transceivers
- ▼ Cable Modems
- ▼ WLAN Transceivers
- ▼ Rapid Prototyping
- ▼ SOPC Development

Name	Description
Digital IF Receiver	The Digital IF Receiver translates the input IF signal down to baseband by utilizing a quadrature NCO and a digital mixer. A pair of Cascaded Integrator Comb (CIC) filters, and FIR filters provide the decimation and bandlimiting to accommodate a wide range of signal bandwidths. The Digital IF Receiver, which is designed to accept data samples up to 16-bits wide, renders complex baseband samples.
Digital Modulator	The Digital Modulator, containing a parameterized complex multiplier/mixer and quadrature output NCO, accepts baseband data and translates it to an IF carrier frequency. The NCO is LUT-based, and has a quadrature output, phase accumulator, and a phase offset input port. The complex multiplier/mixer multiplies two user-defined inputs with the NCO outputs for amplitude modulation or frequency up conversion.
Adaptive Equalizer	The Adaptive Equalizer adapts its own filter response to remove the effects of multipath and other signal degradations. Using the Constant Modulus Algorithm, no training sequence or demodulator decisions are needed. Taps are Read/Write to accommodate multiple transmitters in TDMA systems.
Dual Constraint Length Viterbi Decoder	The Dual Constraint Length Viterbi Decoder provides decoding for the following a variety of modes, including: k=7, rate 1/2; punctured k=7, rate 3/4; punctured k=7, rate 7/8; and k=9, rate 3/4. Both soft decision and hard decision decoding are supported in either sign/magnitude or two's complement format. The decoder can be operated in a synchronous manner through the use of the SOM (start-of-message) signal, or can be self-synchronized by selecting the autosync feature.
Early/Late Gate Symbol Synchronizer	The Early/Late Gate Symbol Synchronizer contains all the functions necessary for a complete, first-order, closed-loop synchronizer. The synchronizer core includes a phase detector, an up-down counter loop filter, and a digitally controlled oscillator (DCO). The phase detector is a balanced early/late gate, dual integrator design. Programmable step sizes and thresholds are provided to control clock jitter and loop bandwidth.
Binary Pattern Correlator	The Binary Pattern Correlator is a digital correlator that compares the digital pattern stored in the reference pattern register with the data samples stored in the correlator shift register. This IP Core contains the following components: a data shift register, a reference pattern register, a mask register, the correlation array, and the correlation summing network.
Complex Multiplier/Mixer	The Complex Multiplier/Mixer core can multiply two complex numbers or mix two complex signals. The function can be used for vector cross products, vector dot products, up/down frequency conversion, differential phase detection, digital amplitude modulation (AM), and quadrature amplitude modulation (QAM). Nova Engineering will customize the input width, output width, and processing latency of the Complex Multiplier/Mixer at no additional cost.
Numerically Controlled Oscillator	The Numerically Controlled Oscillator (NCO) generates digital sine and cosine waveforms at a programmable periodic rate. The sine and cosine outputs can be adjusted over a wide range of frequencies with a high degree of resolution. Nova Engineering can customize the input and output data width to meet user specifications.
CORDIC Numerically Controlled Oscillator	The CORDIC NCO is based on the Coordinate Rotation Digital Computer algorithm and generates digital sine and cosine waveforms at a programmable periodic rate. The CORDIC algorithm calculates the amplitude of the sine and cosine functions given an input phase angle. The CORDIC NCO is not dependent on ROM Look-Up-Table space. Consequently, the CORDIC NCO can deliver significantly better Spurious Free Dynamic Range (SFDR) than Look-Up-Table based NCO's when used in a PLD.
<p>IP Cores are available for evaluation prior to purchase. Purchase options include either Encrypted Net List or VHDL Source Code.</p>	

More information available on our website. Contact us to discuss custom or OEM configurations.
Nova Engineering, Inc. 1-513-642-3000 or info@nova-eng.com.

