Digital IF Receiver Megafunction

Data Sheet (PN F901SC) **December, 2001, ver. 1.1**

Target Applications:

Narrowband and Wideband Digital Receivers

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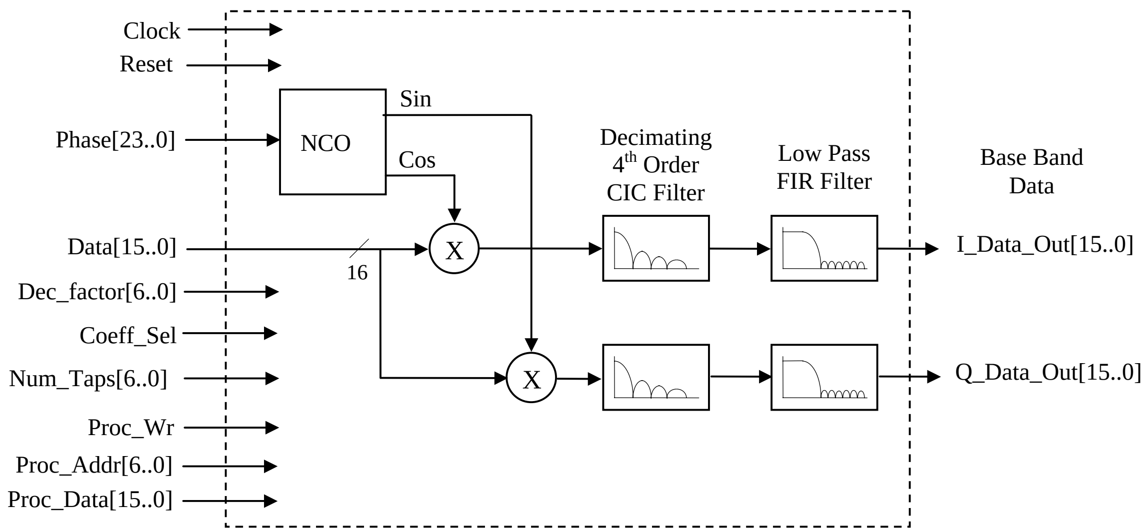
Features

- PLD Provides ASIC Performance plus Software Flexibility
- VHDL Source Code available
- Complete Digital IF Receiver
- Quadrature NCO and Digital Mixer translates IF signal to baseband
- CIC and FIR filters provide decimation and filtering
- Standard processor bus interface supports programmable features

General Description

The Digital IF Receiver megafunction combines a quadrature NCO and a digital mixer to translate the input IF signal down to baseband. A pair of Cascaded Integrator Comb (CIC) filters, and FIR filters provide decimation and bandlimiting to accommodate a range of signal bandwidths. The Digital IF Receiver is designed to input data samples up to 16-bits wide and render complex baseband samples. Consequently the Megafunction uses a quadrature NCO, two digital mixers, two 4th order decimating CIC filters, and two programmable coefficient FIR filters supporting up to 64-taps, to generate both In-phase and Quadrature baseband components.

Figure 1. Digital IF Receiver Megafunction Block Diagram



Detailed Description

The Digital IF Receiver can significantly reduce the processing requirements of DSP-based receivers by pre-selecting the signals of interest and reducing the output sample rate. The reduction in bandwidth and sampling rate can dramatically reduce the cost and complexity of the DSP system used for downstream demodulation or other signal processing.

In addition, the digital signal processing techniques, employed by the Digital IF Receiver, avoid many of the undesirable effects associated with classic analog implementations. For example, digital filters do not require initial component tolerances, calibration or preventive maintenance and do not suffer from temperature variations, or aging characteristics. Digital mixers also eliminate common analog degradation's such as I/Q phase mismatch, amplitude imbalance, and DC offsets.

The Digital IF Receiver Megafunction supports both the classic IF sampling technique as well as IF under-sampling. Through the signal processing technique known as IF under-sampling, images of the desired signal are created at the sampling frequency. This technique can be used with the Digital IF Receiver Megafunction to enable sampling rates below 140MHz for the system A/D converter, while directly sampling a 70MHz IF. When IF under-sampling is used, the Digital IF Receiver allows the bandwidth of interest to be selectively passed while attenuating undesired sampling artifacts.

Table 1 defines the input and output signals of the Digital IF Receiver Megafunction.

Table 1 Interface Signal Definitions

Name	Type	Width	Description
data	Input	16 bits	Periodic samples of the real waveform to be translated in frequency. Two's complement format. Synchronous to rising edge of clock.
phase	Input	24 bits	Data input to tune word register. Two's complement format. Should be updated synchronous to rising edge of clock.
dec_factor	Input	6 bits	Decimation factor, R. Positive integer $3 \le R \le 33$. R must obey the relationship $L = 2(R - 1)$.
coeff_sel	Input	-	0 = FIR reads coefficients (normal operation) 1 = Processor writes coefficients (write coefficients)
num_taps	Input	7 bits	Number of FIR taps, L. Positive, even integer $4 \le L \le 64$. L must obey the relationship $L = 2(R - 1)$.
proc_wr	Input	-	Processor write pulse. Active high. Minimum pulse width is two periods of the master clock.
proc_data	Input	16 bits	Processor data to Coefficient RAM.
proc_addr	Input	7 bits	Processor address to Coefficient RAM. This address is applied to the Coefficient RAM when coeff_sel = 1.
reset	Input	-	Master reset. Active high.
clk	Input	-	Master clock. 50% Duty cycle.
i_data_out	Output	22 bits	In-phase component of complex baseband signal. Two's complement format. Synchronous to clock.
q_data_out	Output	22 bits	Quadrature-phase component of complex baseband signal. Two's complement format. Synchronous to clock.

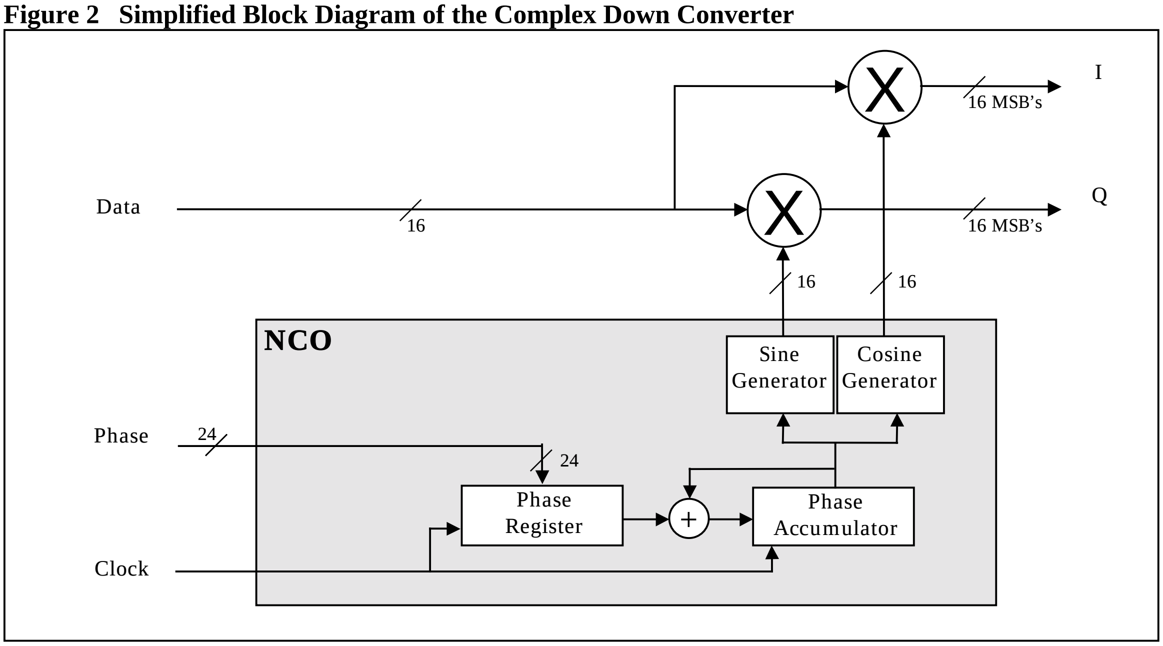
Down Converter Functions

The complex down converter, in the Digital IF Receiver, is designed to translate the spectrum of a sampled bandpass signal from an Intermediate Frequency (IF) down to baseband. This is accomplished by numerically multiplying, or mixing, the real input data samples with the output of a Numerically Controlled Oscillator (NCO).

The NCO is a numerically controlled oscillator, which generates digital sine and cosine waveforms. The frequency of the sine and cosine outputs can be controlled numerically and adjusted with very fine resolution, over a wide range of frequencies. The sine and cosine waveforms, generated by the NCO, have the same frequency but a quadrature phase alignment, or a 90 degree phase difference in time.

The samples received from the A/D are real and periodic at the NCO clock rate. Each sample from the A/D converter is multiplied with the quadrature NCO outputs, as shown in Figure 2, to produce a complex signal pair, I and Q, with each rising edge of the clock.

Figure 2 Simplified Block Diagram of the Complex Down Converter



NCO Operation

The NCO contains sine and cosine generators which can be viewed simply as ROM-based Look Up Tables (LUT) that perform the following functions:

$$\sin[n] = \sin[2\pi n/N]$$
$$\cos[n] = \cos[2\pi n/N]$$

where:
- n = Address input to the LUT
- N = Number of samples in the LUT
- $\sin[n]$ = Amplitude of sine function at $[2\pi n/N]$
- $\cos[n]$ = Amplitude of cosine function at $[2\pi n/N]$.

Incrementing n from 0 to N-1 causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The value $2\pi n/N$ represents a fractional phase angle between 0 and 2π. The time required to increment n from 0 to N-1 is the period of the sine and cosine waveforms produced.

The LUT address is incremented once each cycle of the clock by an amount equal to the phase word input. The phase angle is accumulated and stored in the phase accumulator register. The output of the phase accumulator is used to address the sine and cosine LUT's.

The frequency of the sine and cosine waveforms is given by f, where f is defined as follows:

$$f = fclk * phase[23..0] / 2^{24}$$

where:
- f = Frequency of the sine and cosine waveforms
- fclk = Frequency of the input Clock
- phase[23..0] = 24-bit tune data.

The frequency tuning resolution is given by:

$$\text{frequency resolution} = \pm ½ (fclk / 2^{24}).$$

For example, if fclk = 25MHz, then the frequency resolution = ± 0.75Hz.

Multiplier/Mixer Operation

Two digital multipliers are used to heterodyne, or mix, the input data samples with the NCO quadrature waveforms. The resulting frequency translation can be expressed by the Fourier frequency shifting property shown as a Fourier pair below.

$$x(t)\, e^{j\omega_o t} \Leftrightarrow X(\omega-\omega_o)$$

More specifically,

$$x(t) \cos(2\pi f_o t) = ½ [x(t)\, e^{j2\pi f_o t} + x(t)\, e^{-j2\pi f_o t}] \Leftrightarrow ½ [X(f - f_o) + X(f + f_o)]$$
$$x(t) \sin(2\pi f_o t) = ½j [x(t)\, e^{j2\pi f_o t} - x(t)\, e^{-j2\pi f_o t}] \Leftrightarrow ½j [X(f - f_o) - X(f + f_o)]$$

By multiplying the input data, x(t), by the quadrature sine and cosine waveforms, we achieve a frequency translation of f_o . The multipliers are 16 x 16 bit signed multipliers. The lower 16-bits, of the 32-bit output, is truncated and the 16 most significant bits are used for subsequent processing. The multiplier inputs and outputs are two's complement format.

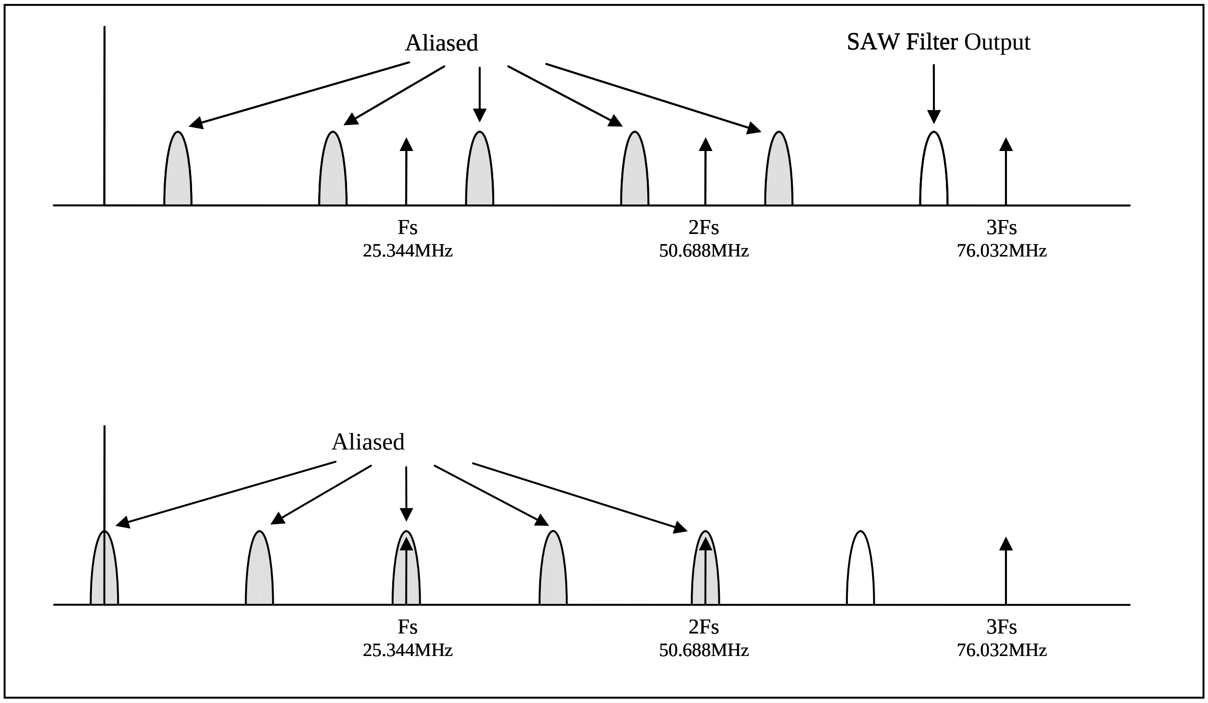
Down Conversion Example

Figure 3 illustrates the frequency down conversion process using IF undersampling. In this example, the A/D converter is operated at a 25.344MHz sampling rate. This rate is below the desired signal of interest, so we must be very careful to choose an A/D converter with an IF undersampling capability, suitable for this application example.

The A/D samples the bandlimited signal presented at the output of the bandpass Surface Acoustic Wave (SAW) Filter. The signal of interest is centered at an IF of 70MHz. The A/D sampling action will produce aliased images of the SAW output, centered around the sampling frequencies nFs, where n = 0,1,2,3,4,etc. Notice the lowest positive frequency image is centered at 6.032MHz.

The second illustration in Figure 3 shows the result of the signal spectrum after down conversion, i.e. frequency translation. In this specific example, the NCO is tuned to 6.032Mhz. When the A/D samples are mixed, or multiplied with the NCO output, the entire spectrum is shifted, or slid, down in frequency by 6.032MHz. The IF undersampling and downconversion process have translated the signal of interest (a purely real signal located at 70MHz) down to baseband (a complex signal located at 0Hz).

Figure 3 Example of Frequency Down Conversion



Filter Functions

The Digital IF Receiver Megafunction contains two filter types. The Cascaded Integrator Comb (CIC) filters are used primarily to reduce the sample rate. The sample rate is decreased by the decimating action of the CIC. The CIC filters support a range of decimation rates, R, from 3 to 33. In addition to decimation, the CIC filters also provide a low pass frequency characteristic as shown in Figure 5. The frequency response of the CIC varies only with the decimation rate, R.

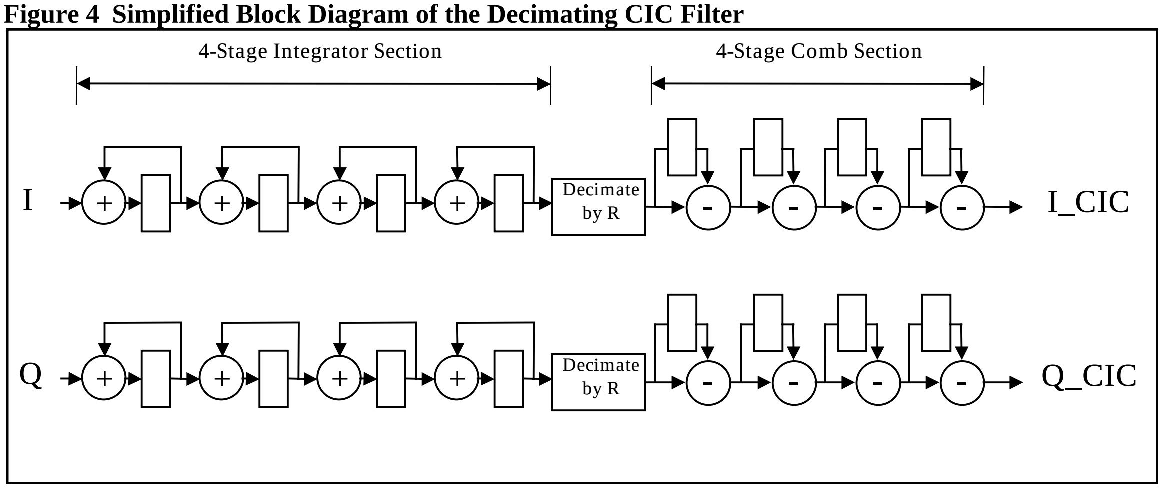
The Finite Impulse Response (FIR) filters are used primarily for isolating the signal of interest by attenuating out-of-band signal energy. The coefficients of the FIR filter are programmable, but the number of taps is coupled to the CIC decimation rate.

CIC Filter Details

The CIC filter is designed to be an economical alternative to the conventional, linear phase, Finite Impulse Response, filter. The CIC filter does not require any multipliers and is therefore useful at high sampling rates, however its filtering characteristics are severely limited. The essential function of the decimating filter is to decrease the sampling rate and to keep passband aliasing within specified limits.

The decimating CIC filter is composed of three functions. The integrator section, which consists of digital integrators operating at the high speed input sampling rate. A rate change, or decimation, section follows the integrator section. The decimated samples feed into the comb filter section. Figure 4 shows a simplified block diagram of the 4-stage, decimating CIC filter.

Figure 4 Simplified Block Diagram of the Decimating CIC Filter



The CIC filter provides the primary low-pass selectivity and reduces the sampling rate, and the complexity, for subsequent processing. The integrator section operates at the A/D sampling rate. Each integrator stage stores the result from the adder and sums it with the new sample. The comb section operates at the sample rate divided by R. Each comb stage subtracts the previous result from the current result.

CIC Operation

The CIC filter suffers from register overflow because of the unity feedback at each integrator stage. The overflow is of no consequence as long as the following two conditions are met:

1) the filter is implemented with two's complement arithmetic
2) the range of the number system is greater than or equal to the maximum value expected at the output

The Digital IF Receiver, CIC Filter, meets both criteria. The CIC filter is chosen because; it requires no multipliers; it requires no filter coefficient storage; intermediate storage is reduced by integrating at the high speed sampling rate and comb filtering at the lower, decimated, rate; the structure of the CIC consists of two simple blocks; little external timing and control are needed; and the same filter permits a wide selection of decimation rates.

The limiting factors of the CIC filter are; registers can become large for large decimation rates; and the frequency response is fully determined by only three parameters (R,M,N), resulting in a limited range of filter characteristics. In the Digital IF Receiver, M is fixed at 1 and N is fixed at 4.

The system function for the CIC filter, referenced to the high speed sampling rate, is found by combining the transfer function of the integrator and comb sections.

$$H(z) = (1-z^{-RM})^N / (1-z^{-1})^N = \left[\sum_{K=0}^{RM-1} z^{-k} \right]^N$$

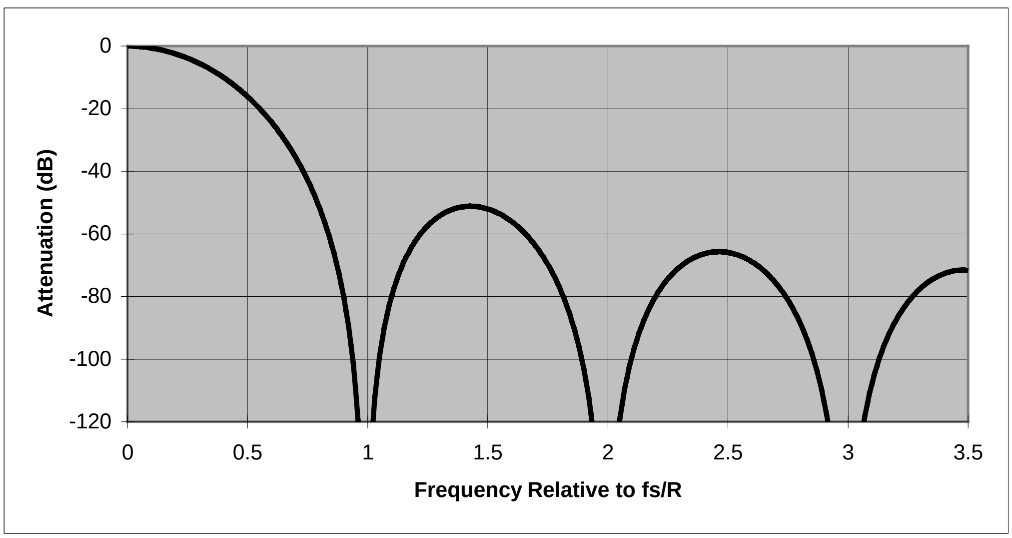
where: N is the number of stages = 4
R is the decimation factor = [3 to 33]
M is the differential delay = 1

The CIC filter has a low pass frequency characteristic evaluated at $e^{j(2\pi f/R)}$, where f is the frequency relative to the decimated rate, f_S/R. The power response for the CIC filter is given by

$$P(f) = [\sin(\pi M f) / \sin(\pi f/R)]^{2N}$$

Figure 5 illustrates the CIC frequency response for N=4, M=1, and R=8.

Figure 5 Frequency Response of Decimating CIC Filter



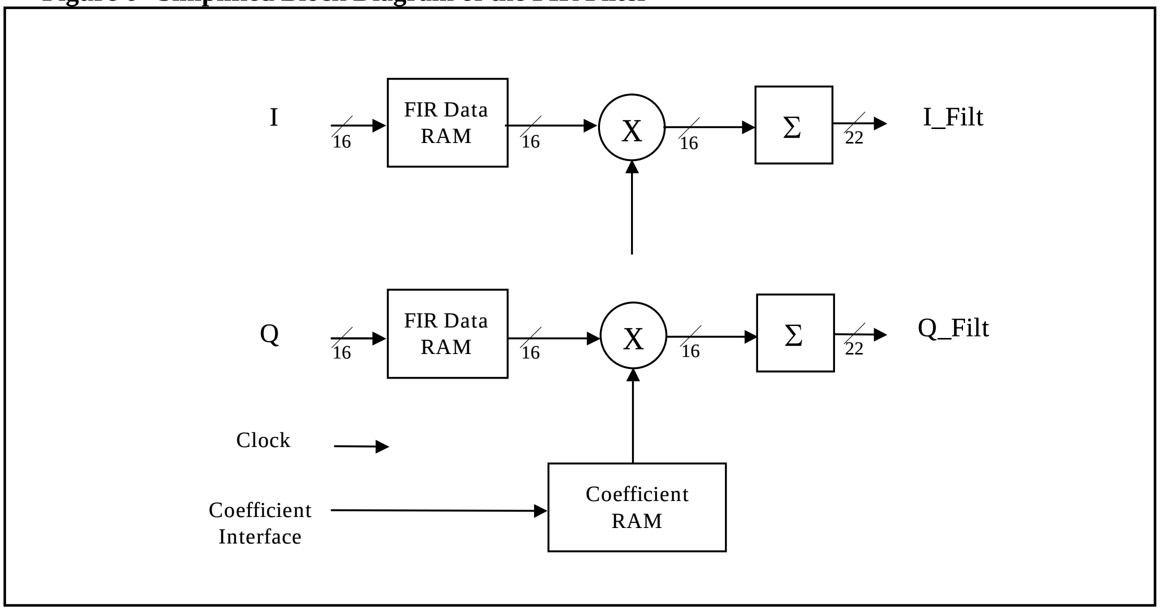
Refer to IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, April 1981, “An Economical Class of Digital Filters for Decimation and Interpolation” by Eugene Hogenauer, for a detailed discussion of CIC filters.

FIR Filter Details

The FIR filter architecture supports up to 64-taps that provide frequency selectivity, with a flat pass band and a linear phase response. The filter pass band, and stop band, are shaped by the programmable filter coefficients

The FIR filter provides low-pass selectivity, for subsequent processing. The filter processes samples at the decimated sample rate. The FIR coefficients determine the frequency selectivity of the filter.

Figure 6 Simplified Block Diagram of the FIR Filter



FIR Operation

The FIR Filter has three basic interfaces; input data samples, coefficient RAM interface, and output data samples. Figure 6 shows a simplified block diagram of the FIR Filter. The FIR filter operates at the master clock rate, but processes samples at the decimated rate. This architecture allows programmable coefficients, but requires multiple clock cycles for each output sample.

The FIR filter performs the following calculation for each output sample, y[k];

$$y[k] = \sum_{n=0}^{N} (x[n] + x[2N + 1 - n]) * h[N - n]$$

where: $N = (L/2) - 1$; $4 \le L \le 64$; L is an even integer.
L represents the number of taps in the FIR filter
h[ ] represents the array of FIR coefficients
x[ ] represents the input sample array
y[ ] represents the FIR output sample array

The FIR filter architecture requires coefficient symmetry. This means h[0] = h[L-1], h[1] = h[L-2], etc. During each clock cycle, the data samples x[n] and x[2N + 1 – n] are summed together first and then multiplied by the same coefficient. This calculation method cuts the number of multiplies in half, and reduces the processing time required for each FIR output, y[k].

For example, (x[0]*h[0] + x[63]*h[63]) = (x[0]+x[63]) * h[0] if h[0]=h[63] (coefficient symmetry)

Also note the FIR coefficients, h[n], are indexed in reverse order. This requires the user to store the coefficients in the coefficient RAM in reverse indexed order. In other words, h[0] should be stored at address 31, h[1] should be stored at address 30, etc., until h[31], which should be stored at address 0.

For example, a 64 tap symmetrical FIR filter has 32 unique coefficients, L=64 and N=31. The FIR calculations proceed as follows:

(x[0] + x[63]) * h[31] ; n=0
(x[1] + x[62]) * h[30] ; n=1
.
(x[30] + x[33]) * h[1] ; n=30
(x[31] + x[32]) * h[0] ; n=31

In this particular example, each FIR output value, y[k], takes 33 clock cycles to complete. Note also that the CIC decimation rate, R, is related to the FIR length, L, by the following equation:

$$L = 2(R - 1) \qquad \text{and} \qquad 3 \le R \le 33.$$

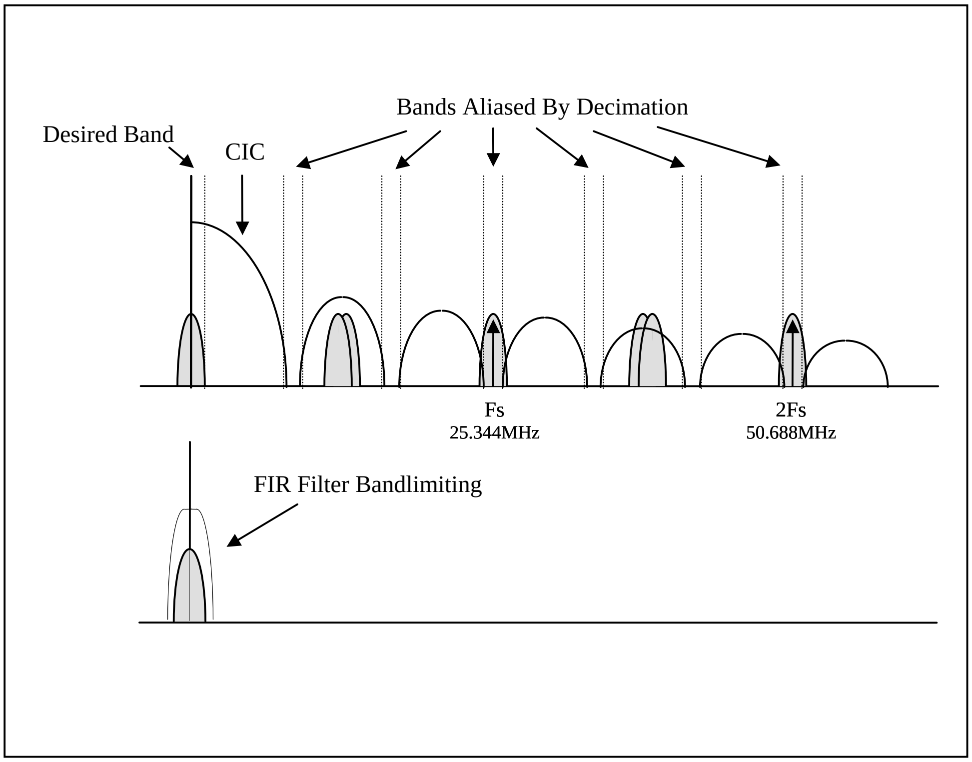
The Digital IF Receiver requires the user to input the decimation rate, R, and the number of taps for the FIR, L. Proper operation requires the user to adhere to the relationship, L = 2(R-1), calculated in Table 2.

Table 2 FIR Length versus Decimation Rate

FIR Taps L	Dec Rate R	Number of FIR Coefficients
64	33	32
62	32	31
60	31	30
58	30	29
56	29	28
54	28	27
52	27	26
50	26	25
48	25	24
46	24	23
44	23	22
42	22	21
40	21	20
38	20	19
36	19	18
34	18	17
32	17	16
30	16	15
28	15	14
26	14	13
24	13	12
22	12	11
20	11	10
18	10	9
16	9	8
14	8	7
12	7	6
10	6	5
8	5	4
6	4	3
4	3	2

Figure 7 illustrates the resulting spectrum after the decimated samples have been down converted and passed through the CIC and FIR filters. The A/D sampling and CIC filters produce a number of alaised images that represent interference to the signal of interest. The FIR filter provides a narrow, low pass response to attenuate and effectively eliminate signals outside the band of interest.

Figure 7 Results of Bandlimiting using CIC and FIR Filter



The FIR coefficients can be programmed via the simplified processor interface. The Digital IF Receiver provides a single control line, coeff_sel, that enables the processor to write into the coefficient RAM. The processor data, proc_data[15..0], and address, proc_addr[6..0], and the processor write, proc_wr, signals are used to transfer user specified coefficients into the FIR coefficient RAM.

Note that coefficients are stored in reverse order, such that h[0] is stored at address 31 for a 64 tap filter, and h[31] is stored at address 0. For a 12 tap filter, there would be 6 unique coefficients. Again the coefficients should be stored in reverse order, such that h[5] is stored at address 0 and h[0] is stored at address 5. All other coefficients should be set to a value of zero.

In addition, the processor write pulse must be at least 2 clock cycles wide. The coefficient RAM is a synchronous Ram that operates at the master clock rate. The processor write, when coeff_sel is set to a logic ‘1’, acts as an enable for the RAM ‘write’ operation. RAM data is actually stored on the rising edge of the clock.

Processing Gain

The A/D samples are subjected to gain changes as they are processed through the Digital IF Receiver. These gain changes are deterministic and include the CIC gain, and the FIR gain. The gain for the 4th order CIC decimator is given as:

$G = (R)^4 / (2^{(W-16)})$;where R is the decimation rate and W = the bit width required to represent the output.

The CIC pass band gain for each decimation rate, R, is listed in Table 3.

Table 3 CIC Gain versus Decimation Rate

R	Gain	R	Gain	R	Gain	R	Gain
1	1	17	0.637215	33	0.565491	49	0.687218
2	1	18	0.800903	34	0.637215	50	0.745058
3	0.632813	19	0.99427	35	0.715554	51	0.806475
4	1	20	0.610352	36	0.800903	52	0.871613
5	0.610352	21	0.741886	37	0.89367	53	0.940619
6	0.632813	22	0.893616	38	0.99427	54	0.506822
7	0.586182	23	0.533754	39	0.551567	55	0.54542
8	1	24	0.632813	40	0.610352	56	0.586182
9	0.800903	25	0.745058	41	0.673714	57	0.629187
10	0.610352	26	0.871613	42	0.741886	58	0.674516
11	0.893616	27	0.506822	43	0.815106	59	0.722251
12	0.632813	28	0.586182	44	0.893616	60	0.772476
13	0.871613	29	0.674516	45	0.977665	61	0.825276
14	0.586182	30	0.772476	46	0.533754	62	0.880738
15	0.772476	31	0.880738	47	0.581703	63	0.93895
16	1	32	1	48	0.632813	64	1

The FIR filter gain is dependent upon the sum of the coefficients, and the number of filter taps. The FIR filter processes each product (x[n] * h[n]) to produce a 32 bit result, that is then truncated to 16 bits. In an N-tap filter, N of these products are accumulated, resulting in a bit growth of $\log_2(N)$, in the accumulator. For example, a 64-tap filter, using 16-bit data, will produce $\log_2(64) = 6$ bits of growth, potentially requiring 22 bits to represent the final result. Depending on the sum of the coefficients, the final result may, or may not grow by the full 6 bits.

IN conclusion, the gain of the Digital IF Receiver varies, with each specific application, because of the decimation rate, the FIR filter length and the coefficient scaling. For this reason the Digital IF Receiver Megafunction provides 22 bits of output, allowing the user to control the system gain by; scaling FIR coefficients and choosing the best range of output bits.

Synthesis Results

The device utilization and performance, of the Digital IF Receiver Megafunction, are dependent upon several factors, such as device family, speed grade, synthesis style and optimization. The following synthesis results were generated using the Quartus II compiler.

Device Utilization Example

Device	SpeedGrade	Utilization		Performance	Parameter Setting
		Logic Cells	ESBs		
20K400E	-1x	5855	28672 bits	70 MHz	16-bit input data samples